SEG CHASSIS 11AK28

MODEL

SERVICE MANUAL

CONTENTS

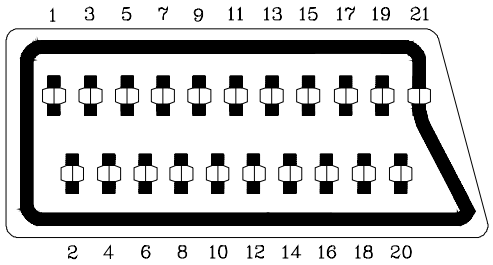
DO NOT CHANGE ANY MODULE UNLESS THE SET IS SWITCH OFF
The mains supply side of the switch mode power supply transformer is live.
Use an isolating transformer.
The receivers fulfill completely the safety requirements.

Safety precautions:
Servicing of this TV should only be carried out by a qualified person.
- Components marked with the warning symbol on the circuit diagram are critical for safety and must only be replaced with an identical component.
- Power resistor and fusable resistors must be mounted in an identical manner to the original component.
- When servicing this TV, check that the EHT does not exceed 26kV.

TV Set switched off:
Make short-circuit between HV-CRT clip and CRT ground layer.
Short C804 (150mF) before changing IC802 or other components in primary side of SMPS.

Measurements:
Voltage readings and oscilloscope traces are measured under following conditions.
Antenna signal 60dB from colourbar generator. (100% white, 75% colour saturation)
Brightness, contrast, colour set for a normal picture.
Mains supply, 220VAC, 50Hz.

PERI-TV SOCKET



	SCART 1 (SC050)		SCART 2 (SC051)	
1	Audio right output	0.5Vrms / 1K	Audio right output	0.5Vrms / 1K
2	Audio right input	0.5Vrms / 10K	Audio right input	0.5Vrms / 10K
3	Audio left output	0.5Vrms / 1K	Audio left output	0.5Vrms / 1K
4	Ground AF		Ground AF	
5	Ground Blue		Ground Blue	
6	Audio left input	0.5Vrms / 10K	Audio left input	0.5Vrms / 10K
7	Blue input	0.7Vpp / 75ohm	Blue input	0.7Vpp / 75ohm
8	AV switching input	0-12VDC /10K	AV switching input	0-12VDC /10K
9	Ground Green		Ground Green	
10	-		-	
11	Green input	0.7Vpp / 75ohm	-	
12	-		-	
13	Ground Red		Ground Red	
14	Ground Blanking		Ground Blanking	
15	Red input	0.7Vpp / 75ohm	-	
16	Blanking input	0-0.4VDC, 1-3VDC / 75ohm	-	
17	Ground CVS output		Ground CVS output	
18	Ground CVS input		Ground CVS input	
19	CVS output	1Vpp / 75ohm	CVS output	1Vpp / 75ohm
20	CVS input	1Vpp / 75ohm	CVS input	1Vpp / 75ohm
21	Ground		Ground	

INTRODUCTION

11Ak28 is a 100Hz flicker free colour television capable of driving 28”4:3/16:9, 33”4:3 and 29”4:3 real flat picture tubes. The chassis is capable of operation in PAL, SECAM, NTSC (playback) colour standards and multiple transmission standards as B/G, D/K, I/I’, and L/L´.Sound system output is supplying 12W (10%THD) for left, right and center outputs of 8ohm speakers, and 2 x 7W for surround outputs of 2 x 4ohm speakers, connected in series.

TV supports the hightext (level 2.5) teletext standard. It is possible to decode transmissions including high graphical data. The chassis is equipped with one full EuroScart, two other SCARTs for AV input/output, one front-AV input, one back-AV output, one headphone output, one SVHS input (via SCART and SVHS connector), one VGA input, two external speaker outputs (left and right), one centre speaker output, and one surround speaker output for two speakers in series.

POWER SUPPLY (SMPS)

TDA16846

A SMPS transformer controlled by the IC TDA16846, which is designed for driving, controlling, and protecting switching transistor, provides the DC voltages required at various parts of the chassis. SMPS generates the necessary 5V supply for the micro-controller, 130V supply for the FBT, +/-16V supply for the audio amplifier, which are active in stand-by and others 8V, 12V and 5V for other different parts of the chassis.

When the TV is switched on, a reference voltage is provided to TDA16846 and the start-up operation occurs, then TV enters into the stand-by position.

Two optocouplers are used to control the regulation of line voltage and stand-by power consumption. There are two regulation circuits, one in primary side and one in secondary side. The primary regulation circuit provides a control voltage to pin3 of the IC. Secondary regulation circuit produces a control voltage according to the changes in 130V DC voltage, via an optocoupler (SFH617A) to pin4 of the IC.

During the switch on period of the transistor, energy is stored in the transformer. During the switch off period energy is fed to the load via secondary winding. By varying switch-on time of the power transistor, it controls each portion of energy transferred to the second side such that the output voltage remains nearly independent of load variations. At the same time, the supply voltages 12V, 8V, 5V are stabilised by the series regulators.

Features:

- Line Current Consumption with PFC
- Continuous Frequency Reduction with Decreasing Load
- Stable and Adjustable Stand-by Frequency
- Very Low Start-up Current
- Soft-Start for Quiet Start-up
- Adjustable and Voltage Dependent Ringing Suppression Time
- Synchronization and Fixed Frequency Facility
- Over- and Under-voltage Lockout
- Switch Off at Mains Under-voltage
- Mains Voltage Dependent Fold Back Point Correction
- Low Power Consumption
- Free usable Fault Comparators

Pinning:

1. OTC Off Time Circuit
2. PCS Primary Current Simulation
3. RZI Regulation and Zero Crossing Input
4. SRC Soft-Start and Regulation Capacitor
5. OCI Opto Coupler Input
6. FC2 Fault Comparator 2
7. SYN Synchronization Input
8. N. C. Not Connected
9. REF Reference Voltage and Current
10. FC1 Fault Comparator 1
11. PVC Primary Voltage Check
12. GND Ground
13. OUT Output
14. VCC Supply Voltage

IF PART

TDA4470 / TDA4472

The TDA44XX is an integrated bipolar circuit for multistandard video/sound IF (VIF/SIF) signal processing in TV/VCR and multimedia applications. The circuit processes all TV video IF signals with negative modulation (e.g., B/G standard), positive modulation (e.g., L standard) and the AM, FM/NICAM sound IF signals. Active carrier generation by FPLL (frequency phase-locked loop) is the principle for true synchronous demodulation. VCO circuit is operating on picture carrier frequency, the VCO frequency is switchable for L´-mode. AFC without external reference circuit is alignment-free and polarity of the AFC curve is switchable. VIF-AGC for negative modulated signals operates on peak sync detection principle and for positive modulation on peak white / black level detection principle. Tuner AGC is adjustable with determining take over point. It has alignment-free quasi-parallel sound (QPS) mixer for FM/NICAM sound IF signals. Intercarrier output sound is gain controlled (necessary for digital sound processing). AM-demodulator is completely alignment-free with gain controlled AF output. Operation of the AM demodulator and QPS mixer (for NICAM-L stereo sound is parallel. TDA4472 is used for negative modulation and TDA4470 is used for both negative and positive modulation.

Features:

- 5V supply voltage; low power consumption
- Active carrier generation by FPLL principle (frequency-phase-locked-loop) for true synchronous demodulation
- Very linear video demodulation, good pulse response and excellent intermodulation figures
- VCO circuit is operating on picture carrier frequency, the VCO frequency is switchable for the L' mode
- Alignment-free AFC without external reference circuit, polarity of the AFC curve is switchable
- VIF-AGC for negative modulated signals (peak sync detection) and for positive modulation (peak white/black level detector).
- Tuner AGC with adjustable take over point
- Alignment-free quasi parallel sound (QPS) mixer for FM/NICAM sound IF signals
- Intercarrier output signal is gain controlled (necessary for digital sound processing)
- Complete alignment-free AM demodulator with gain controlled AF output
- Separate SIF-AGC with average detection
- Two independent SIF inputs
- Parallel operation of the AM demodulator and QPS mixer (for NICAM-L stereo sound)
- Package and relevant pinning is compatible with the single standard version TDA 4472;simplifies the design of an universal IF module

Pinning:

1.	Input sensitivity, RMS value	: 80mVrms
2.	Input sensitivity, RMS value	: 80mVrms
3.	SIF Input selector switch	: 2.0 V
4.	Ground	
5.	IF gain control range	: 65dB
6.	Input sensitivity, RMS value	: 80mVrms
7.	Input sensitivity, RMS value	: 80mVrms
8.	IF gain control range	: 65dB
9.	Ground	
10.	Available tuner-AGC current	: 2mA
11.	Available tuner-AGC current	: Min : 0.3V Max : 13.5V
12.	Video output	: Min : 1.8V Max : 2.2V
13.	Standard switch	: Min : 0V Max : 0.8V
14.	L' switch	: Min : 0V Max : 3.0V
15.	IF gain control range	: 65dB
16.	Ground	
17.	Internal reference voltage	
18.	FPLL and VCO	: Min : 1mA Max : 4mA
19.	AFC switch	: Min : 0V Max : 0.8V
20.	FPLL and VCO	: Min : 1mA Max : 4mA
21.	FPLL and VCO	: Min : 1mA Max : 4mA
22.	AFC output	: 0.7 mA/kHz
23.	DC supplay	: Min : 4.5V Max : 9.0V
24.	DC output voltage	: 2V
25.	AF output-AM	: 2.2V
26.	FPLL and VCO	: Min : 1mA Max : 4mA
27.	Input sensitivity, RMS value	: 80mVrms
28.	Input sensitivity, RMS value	: 80mVrms

TUNER

The hardware and software of the TV is suitable for tuners, supplied by different companies, which are selected from the Service Menu. These tuners can be combined VHF, UHF tuners suitable for CCIR systems B/G, H, L, L´, I/I´, and D/K. The tuning is available through the digitally controlled I2C bus (PLL). Below you will find info on one of the Tuners in use.

General description of UV1316:

The UV1316 tuner belongs to the UV 1300 family of tuners, which are designed to meet a wide range of applications. It is a combined VHF, UHF tuner suitable for CCIR systems B/G, H, L, L', I and I'. The low IF output impedance has been designed for direct drive of a wide variety of SAW filters with sufficient suppression of triple transient.

Features of UV1316:

- Member of the UV1300 family small sized UHF/VHF tuners
- Systems CCIR: B/G, H, L, L', I and I'; OIRT: D/K
- Digitally controlled (PLL) tuning via I2C-bus
- Off-air channels, S-cable channels and Hyperband
- World standardised mechanical dimensions and world standard pinning
- Compact size
- Complies to "CENELEC EN55020" and "EN55013"

Pinning:

1. Gain control voltage (AGC) : 4.0V, Max:4.5V
2. Tuning voltage
3. I²C-bus address select : Max:5.5V
4. I²C-bus serial clock : Min:-0.3V, Max:5.5V
5. I²C-bus serial data : Min:-0.3V, Max:5.5V
6. Not connected
7. PLL supply voltage : 5.0V, Min:4.75V, Max:5.5V
8. ADC input
9. Tuner supply voltage : 33V, Min:30V, Max:35V
10. Symmetrical IF output 1
11. Symmetrical IF output 2

SAW FILTERS

K9453: Two channels switchable sound IF saw filter of BG, DK, I, L systems for input channel 2 and of L´ system for input channel 1.
K3953: Two channel switchable video IF saw filter of BG, DK, I, L systems for input channel 2 and of L´ system for input channel 1.
J3950: Video IF saw filter for I system

DIGITAL TV SOUND PROCESSING

MSP3410D

The MSP3410D is an I2C controlled single-chip multistandard sound processor for applications in analog and digital TV sets. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out is performed in a single-chip covering all European TV-standards. It is designed to simultaneously perform digital demodulation and decoding of NICAM-coded TV stereo sound, as well as demodulation of FM-mono TV sound and two FM systems according to the German or Korean terrestrial specs. It is also possible to do AM-demodulation according to the SECAM system. There is AGC for analog inputs: 0.14 - 3Vpp. All demodulation and filtering is performed on chip and is individually programmable. All digital NICAM standards (B/G, L, and I) are realised. Only one crystal clock (18.432Mhz) is necessary. External capacitors at each crystal pin to ground are required. They are necessary for tuning the open-loop frequency of the internal PLL and for stabilising the frequency in closed-loop operation. The higher the capacitors, the lower the clock frequency result. The nominal free running frequency should match the centre of the tolerance range between 18.433 and 18.431Mhz as closely as possible. By means of standardised I2S interface, additional feature processors (DPL35xx, Dolby Prologic processor for this chassis) can be connected to the IC.
I2S bus interface consists of five pins:

I2S_DA_IN1…2	for input four channels (two channels per line) per sampling cycle (32Khz).
I2DA_OUT,	for output, two channels per sampling cycle (32KHz).
I2S_CL,	for timing of the transmission of I2S serial data, 1.024Mhz.
I2S_WS,	for the word strobe line defining the left and right sample.

Features:

- 5-band graphic equalizer (as in MSP3400C)
- Enhanced spatial affect (pseudo stereo / base-width enlargement as in MSP3400C)
- Headphone channel with balance, bass treble, loudness
- Balance for loudspeaker and headphone channels in dB units (optional)
- Additional pair of D/A converters for SCART2 out
- Improved over-sampling filters (as in MSP 3400C)
- Additional SCART input
- Full SCART in/out matrix without restrictions
- SCART volume in dB units (optional)
- Additional I²S input (as in MSP 3400C)
- New FM-identification (as in MSP 3400C)
- Demodulator short programming
- Auto-detection for terrestrial TV-sound standards
- Precise bit-error rate indication
- Automatic switch from NICAM to FM/AM or vice versa
- Improved NICAM synchronisation algorithm
- Improved carrier mute algorithm
- Improved AM-demodulation
- ADR together with DRP 3510A
- Dolby Pro Logic together with DPL 35xx A
- Reduction of necessary controlling
- Less external components
- Significant reduction of radiation

Pinning:

1. ADR wordstrobe
2. Not connected
3. ADR data output
4. I²S 1 data input
5. I²S data output
6. I²S wordstrobe
7. I²S clock
8. I²S data
9. I²S clock
10. Not connected
11. Standby (low-active)
12. I²C Bus address select
13. Digital control output 0
14. Digital control output 1
15. Not connected
16. Not connected
17. Not connected
18. Audio clock output
19. Not connected
20. Crystal oscillator
21. Crystal oscillator
22. Test Pin
23. IF input 2 (if ANA_IN1+is used only, connect
24. IF common
25. IF input 1
26. Analog power supply +5V
27. Analog ground
28. Mono input
29. Reference voltage IF A/D converter
30. Scart input 1 in, right
31. Scart input 1 in, left
32. Analog Shield Ground 2
33. Scart input 2 in, right
34. Scart input 2 in, left
35. Analog Shield Ground 1
36. Scart input 3 in right
37. Scart input 3 in left
38. Analog Shield Ground 4
39. Scart input 4 in, right
40. Scart input 4 in, left
41. Not connected
42. Analog reference voltage high voltage part
43. Analog ground
44. Volume capacitor MAIN
45. Analog power supply 8.0V
46. Volume capacitor AUX
47. Scart output 1, left
48. Scart output 1, right
49. Reference ground 1 high voltage part
50. Scart output 2, left
51. Scart output 2, right
52. Analog Shield Ground 3
53. Not connected
54. Not connected
55. Not connected
56. Analog output MAIN, left
57. Analog output MAIN, right to AVSS with 50 pF capacitor) 58.
58. Reference ground 2 high voltage part
59. Analog output AUX, left
60. Analog output AUX, right
61. Power-on-reset
62. Not connected
63. Not connected
64. Not connected
65. I²S2-data input
66. Digital ground
67. Digital power supply +5V
68. ADR clock

DOLBY PRO LOGIC PROCESSOR IC

DPL3519A

The IC DPL3519A processor family is designed to decode Dolby encoded surround sound. The IC integrate the complete Dolby Surround Pro Logic decoding on chip without any necessary external circuitry. It designed as a coprocessor of the MSP34xx family.

It gets digitised sound from the audio processor IC MSP3410D for both C (centre) and S (surround) channels, and for both L (left) and R (right) channels. The analog L and R outputs are supplied by MSP3410D, while the analog S and C outputs are supplied by the DPL33519A.

Two I2S busses obtain synchronisation between the MSP and DPL :

I2S_CL; for timing of the transmission of I2S serial data 1.024Mhz and I2S_WS; The word strobe line defining the left and right sample at 32Khz. The IC is also I2C bus controlled to select the sound feature (Stereo, 3D-Phonic and Dolby Pro Logic).

Pinning:

1. Not connected
2. Not connected
3. Not connected
4. I2S1 data input
5. I2S1 data output
6. I2S wordstrobe
7. I2S clock
8. I2C data
9. I2C clock
10. Not connected
11. Standby (low-active)
12. I2C-Bus address select
13. Digital control IO 0
14. Digital control IO 1
15. Not connected
16. Not connected
17. Not connected
18. Audio clock output
19. Digital control input
20. Crystal oscillator
21. Crystal oscillator
22. Test pin
23. Not connected
24. Not connected
25. Not connected
26. Analog power supply +5 V
27. Analog ground
28. Mono input
29. Reference voltage
30. Scart input 1 in, right

31. Scart input 1 in, left
32. Analog Shield Ground 1
33. Scart input 2 in, right
34. Scart input 2 in, left
35. Analog Shield Ground 2
36. Scart input 3 in, right
37. Scart input 3 in, left
38. Analog Shield Ground 4
39. Not connected
40. Not connected
41. Not connected
42. Analog reference voltage high voltage part
43. Analog ground
44. Volume capacitor Channel1
45. Analog power supply 8.0 V
46. Volume capacitor Channel 2
47. Scart output 1, left
48. Scart output 1, right
49. Reference ground 1 high voltage part
50. Scart output 2, left
51. Scart output 2, right
52. Analog Shield Ground 3
53. Not connected
54. Not connected
55. Not connected
56. Analog output Channel 1, left
57. Analog output Channel 1, right
58. Reference ground 2 high voltage part
59. Analog output Channel 2, left
60. Analog output Channel 2, right
61. Power-on-reset
62. Not connected
63. Not connected
64. I2S2-data output
65. I2S2-data input
66. Digital ground
67. Digital power supply +5 V
68. Not connected

HEADPHONE OUTPUT

TDA1308

The TDA1308 is an integrated class AB stereo headphone driver. It gets its input from two analog audio outputs (DACA_L and DACA_R) of MSP3410D. The gain of the output is adjustable by the feedback resistor between the inputs and outputs.

Features:

- Wide temperature range
- No switch ON/OFF clicks
- Excellent power supply ripple rejection
- Low power consumption
- Short-circuit resistant
- High performance - high signal-to-noise ratio
  - high slew rate
  - low distortion
- Large output voltage swing

Pinning:

1. Output A (Voltage swing) : Min : 0.75V, Max : 4.25V
2. Inverting input A : Vo(clip) : Min : 1400mVrms
3. Non-inverting input A : 2.5V
4. Ground
5. Non-inverting input B : 2.5V
6. Inverting input B : Vo(clip) : Min : 1400mVrms
7. Output B (Voltage swing) : Min : 0.75V, Max : 4.25V
8. Positive supply : 5V, Min : 3.0V, Max : 7.0V

AUDIO OUTPUT

TDA7265

The TDA7265 is a 25W+25W stereo sound amplifier with mute/stand-by facility. STPA control signal coming from microcontroller (when it is at high level) activates the mute function. IC is muted when mute port is at low level. Two stereo audio signals coming from audio module is injected to the inputs of the IC and a power of 12Wrms (10%) is obtained. An external pop-noise circuitry pulls AF inputs of the IC in order to eliminate pop noise when TV is turned on or off via mains supply connection. It is possible to adjust the gain of the amplifiers by feedback external resistors.

Features:

- Wide supply voltage range (up to 50V ABS Max.)
- Split supply
- High output power: 25+25 W @ TDA = 10%, RL = 8ohm, VS = ±20V
- No pop at turn-on / off
- Mute (pop free)
- Stand-By feature (low IQ)
- Few external components
- Thermal overload protection
- Adjustable gain via an external resistor

Pinning:
1. Output (1)
2. +Vs
3. Output (2)
4. Mute / St-By
5. -Vs
6. Input (2)
7. Ground
8. Input (1)

VIDEO INPUT AND OUTPUT SOURCE SWITCHING

TEA6415C

Video switching is performed by the I2C controlled IC TEA6415C with a gain of 0dB. Inputs to the video switch are IF_CVBS, three SCART video signals, front-AV video signal, SVHS luma signal, and one of SC1_R or SVHS_C. Outputs of the video switch are three SCART video signals (SC1_OUT_V and SC3_OUT_V are the same), one video output for the PIP module, Chroma signal (C), and luma (Y) or CVBS signal.

Features:
- 20 MHz Bandwith
- Cascadable with another TEA6415C (Internal address can be changed by pin 7 voltage)
- 8 inputs (CVBS, RGB, Mac, CHROMA, …)
- 6 Outputs
- Possibility of MAC or chroma signal for each input by switching-off the clamp with an external resistor bridge
- Bus controlled
- 6.5dB gain between any input and output
- -55dB crosstaljk at 5MHz
- Fully ESD protected

Pinning:

1.	Input	:	Max	: 2Vpp,	Input Current	: 1mA,	Max	: 3mA
2.	Data	:	Low level	: -0.3V	Max	: 1.5V,		
			High level	: 3.0V	Max	: Vcc+0.5V		
3.	Input	:	Max	: 2Vpp,	Input Current	: 1mA,	Max	: 3mA
4.	Clock	:	Low level	: -0.3V	Max	: 1.5V,		
			High level	: 3.0V	Max	: Vcc+0.5V		
5.	Input	:	Max	: 2Vpp,	Input Current	: 1mA,	Max	: 3mA
6.	Input	:	Max	: 2Vpp,	Input Current	: 1mA,	Max	: 3mA
7.	Prog							
8.	Input	:	Max	: 2Vpp,	Input Current	: 1mA,	Max	: 3mA
9.	Vcc	:	12V					
10.	Input	:	Max	: 2Vpp,	Input Current	: 1mA,	Max	: 3mA
11.	Input	:	Max	: 2Vpp,	Input Current	: 1mA,	Max	: 3mA
12.	Ground							
13.	Output	:	5.5Vpp,	Min : 4.5Vpp				
14.	Output	:	5.5Vpp,	Min : 4.5Vpp				
15.	Output	:	5.5Vpp,	Min : 4.5Vpp				
16.	Output	:	5.5Vpp,	Min : 4.5Vpp				
17.	Output	:	5.5Vpp,	Min : 4.5Vpp				
18.	Output	:	5.5Vpp,	Min : 4.5Vpp				
19.	Ground							
20.	Input	:	Max	: 2Vpp,	Input Current	: 1mA,	Max	: 3mA

VIDEO OUTPUT AMPLIFIER STAGE

TDA6111Q

The TDA6111Q is a video output amplifier with 16Mhz bandwidth. It has a high slew rate. Automatic black-current stabilisation is possible by black-current measurement output. It has two cathode outputs: one for DC currents and one for transient currents. A feedback output is separated from the cathode outputs. An internal protection exists against positive appearing cathode-ray-tube flashover discharges with ESD protection.

Features:
- High bandwidth and slew rate
- Black-current measurement output for Automatic Black-current Stabilisation (ABS)
- Two cathode outputs; one for DC currents, and one for transient currents
- A feedback output separated from the cathode outputs
- Internal protection against positive appearing cathode-ray Tube (CRT) flashover discharges
- ESD protection
- Simple application with a variety of colour decoders
- Differential input with a designed maximum common mode input capacitance of 3pF, a maximum differential mode input capacitance of 0.5 pF and a differential input voltage temperature drift of 50 uV/K
- Defined switch-off behaviour.

Pinning:
1. Non-inverting voltage input
2. Supply voltage LOW
3. Inverting voltage input
4. Ground, substrate
5. Black current measurement output
6. Supply voltage HIGH
7. Cathode transient voltage output
8. Cathode CD voltage output
9. Feedback voltage output

VERTICAL OUTPUT STAGE

TDA9379FA

The IC TDA9379FA is the vertical deflection booster circuit. Two supply voltages, +12V and –12V are needed to scan the inputs VERT+ and VERT-, respectively. And a third supply voltage, +45V for the flyback limiting are needed. The vertical deflection coil is connected in series between the output and feedback to the input.

Features:
- Power Amplifier
- Thermal Protection
- Output Current up to 2.6App
- Flyback Voltage up to 90V
- External Flyback Supply

Pinning:
1. Inverting Input
2. Supply Voltage
3. Flyback Supply
4. GND or Negative Supply
5. Output
6. Output Stage Supply
7. Non-inverting Input

MICROTEXT CONTROLLER

SDA30C264

The SDA30C264 is the microcontroller used with the Megatext IC. Its architecture and instruction set are based upon that of the 8051 microcomputer. Like the 8051 it has many features which increase programming ease; extended internal data memory-space, variable manipulation in internal data memory, free stack location in data RAM, 4 register banks, special function registers, memory mapped I/O, individually addressable bits, and a Boolean processor which gives the programmer the ability to improve the power of the software development. The IC produces the following input or output control signals; AGC_CON, MODE_SW, L / L', PIP_MODS, PIP_SEL, ON/OFF (stand-by), SC1..3_IN_AV (pin 8 information from 3 SCARTs), AFC, MUTE (to mute audio output IC), I2CEN.

The SDA30C26x family, a derivative of the SAB C501, is a member of family of single-chip computers, in which the emphasis is no longer placed on purely numeric computational performance, but on application-specific controller functions.
Architecture and instruction set are based upon that of the 8051 microcomputer. Like the 8051 has many features which increase programming ease; extended internal data memory-space, variable manipulation in internal data memory, free stack location in data RAM, 4 register banks, special function registers, memory mapped I/O, individually addressable bits and a Boolean processor give the programmer the ability to improve the power of software development. Numerical problems can be processed with binary as well as with BCD-arithmetic. The many bit handling instructions also contribute to the computer's efficiency as a controller, Extended memory is controlled by an 8-bit data and a (16+3)-bit address bus without any additional devices such as latches or logic elements, even when all 512K of the program address space is used. All this leads, in suitable applications, to a reduction in the peripheral hardware and to a simplification of the software and thus to reduced development and component costs. The controller, specially developed for entertainment electronic applications, can also be recommended where both lowest component costs and a large production volume are prime requirements.
The SDA 30C36x family members contain a 1024 + 256-byte or a 2048 + 256-byte data memory (XRAM + RAM), two independent 16-bit timers /-counters and a seven-source, four-priority-level, nested interrupt structure, on-chip oscillator and clock circuits. The 30 digital I/O-lines include four 8-bit ports (P1 and P3 contain I/O-lines with multifunction options) and one 2-bit port. One or two serial interfaces are included, one behaves like the 8051 UART, the other is a I²C Bus interface (SDA 30C264 only)
The second multifunction port consists of port P1, which alternatively can be used as up to eight independent pulse width modulated output channels (PWM). Controlled via special function registers, the PWM-circuitry provides flexibility in time resolution and system configuration.
Specially the realisation of D/A-outputs using pulse width modulation will be a cost saving advantage in analog applications.

The internal ADC is an 8-bit, four-channel converter. The input channels are P20 to P23, the analog supply are pins VDDA and VSSA. A flexible overvoltage / undervoltage detector is included (SDA 30C264 only).
Port 4 can be used as a standard port or as memory extension address bits.
Increased system reliability can be achieved by activating the integrated watchdog timer.
Efficient use of program memory results from an instruction set consisting of 49 single-byte, 46 two-byte and 16 three-byte instructions. Using an internal clock frequency of 12 MHz, 64 instructions execute in 0.5 us and 45b instructions execute in 1.0us. The remaining instructions (multiple and devide) require only 2us. The number of bytes in each instruction and the number of oscillator periods required for execution are listed in the instruction
Based on the SDA 30C163 and similar to the SDA 30C164, the SDA 30C26x comprise double stack size for the extension memory (32 byte) and seven additional data pointer registers.
The SDA 30C263 is a reduced version of the SDA 30C264. The SDA 30C264 is functionally compatible to the SDA 30C164, but uses a different package and a different Reset input stage (P-MQFP-80-1 instead of P-LCC-84).
If using the P-MQFP-64-1 Package, some I/O-features are not available.

Features:

- **SAB 8051 Architecture**
  - On-chip oscillator and clock circuits
  - Binary or decimal arithmetic
  - Signal-overflow detection and parity computation
  - Integrated Boolean processor for control applications
  - Full depth stacks for subroutines return linkage and data storage
  - Four priority level, nested interrupt structure
  - 0.5us instruction cycle at 12 MHz internal clock rate
  - 8 data pointer registers
- **Serial interface**
  - Full duplex UART-interface
  - I²C compatible interface (SDA 30C264 only)
- **On-Chip RAM**
  - Direct byte and bit addressability
  - Four register banks
  - 256 bytes of data memory, including 128 user-defined software flags
  - 2048 bytes of data memory accessible with MOVX-instructions (SDA 30C263; 1024 bytes)
- **External Program Memory Interface**
  - 512 Kbytes of program memory may be addressed by a 8-bit data bus and a 16 + 3-bit address bus
  - Extension stacks depth 32 byte
- **30 Bi-directional I/O-Lines**
  - Two 8-bit ports, one comprising up to eight programmable D/A-outputs
  - One 4-bit input port, also used for analog input
  - One 8-bit port with open drain output
  - One 2-bit port with optional memory extension function
- **Pulse Width Modulation Unit**
  - Up to eight programmable PWM-output channels for low cost digital-to-analog conversion
- **Timers**
  - Two 16-bit general purpose timer/event counters
  - Watchdog timer
- **Analog-to-Digital Converter**
  - Four multiplexed input channels with 8-bit resolution
  - Overvoltage/Undervoltage Detector with interrupts capability

SERIAL ACCESS 32K EEPROM

24LC32A

It is the 32Kbit electrically erasable programmable memory. The memory is compatible with the I2C standard, two wire serial interface, which uses a bi-directional data bus and serial clock.

Features:

- Single supply with operation down to 2.5V
  - Maximum writes current 3mA at 6.0V
  - Standby current 1mA max at 2.5V
- 2-wire serial interface bus, I 2 CÔ compatible
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Self-timed ERASE and WRITE cycles
- Power on/off data protection circuitry
- Hardware write protect
- 1,000,000 Erase/Write cycles guaranteed
- 32-byte page or byte writes modes available
- Schmitt trigger filtered inputs for noise suppression

- Output slope control to eliminate ground bounce
- 2 ms typical write cycle time, byte or page
- Up to eight devices may be connected to the same bus for up to 256K bits total memory
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP and SOIC packages
- Temperature ranges
  - Commercial (C): 0°C to +75°C
  - Industrial (I): -40°C to +85°C

Pinning:

1. A0 User Configurable Chip Select
2. A1 User Configurable Chip Select
3. A2 User Configurable Chip Select
4. Vss Ground
5. SDA Serial Address/Data I/O
6. SCL Serial Clock
7. WP Write Protect Input
8. Vcc +2.5V to 6.0V Power Supply

DRAM

HYB514400BJ

The HYB514400BJ is the new generation dynamic RAM organised as 1M by 4-bit. It utilises CMOS silicon gate process as well as advances circuit techniques to provide wide operation margins both internally and for the system user. This DRAM is used with Megatext IC to store teletext pages.

Features:

- 1 048 576 words by 4-bit organisation
- 0 to 70 °C operating temperature
- Fast Page Mode Operation
- Single +5V (± 10 %) supply with a built-in VBB generator
- Low power dissipation
  max. 660mW active (-50 version)
  max. 605mW active (-60 version)
  max. 550mW active (-70 version)
- Standby power dissipation
  11mW max. Standby (TTL)
  5.5mW max. Standby (CMOS)
  1.1mW max. Standby (CMOS) for low Power Version
- Output unlatched at cycle and allows two-dimensional chip selection
- Read, writes, read-modify write, CAS-before-RAS refreshes,RAS-only refresh hidden refresh and test mode capability
- All inputs and outputs TTL-compatible
- 1024 refresh cycles / 16 ms
- 1024 refresh cycles / 128 ms Low Power Version only
- Plastic Packages: P-SOJ-26/20-5 with 300mil width

EPROM

ST27C2001

The ST27C2001 is 2097 152-bit, ultra-violet erasable, electrically programmable read-only memory. This device is fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by series 74TTL circuits without the use of external pull-up resistors. Each output can drive one series 74 TTL circuit without external resistors. Software for user interface and control of hardware circuitry are stored in this IC.

Features:

- Organisation ...256K x 8
- Single 5-Vpover supply
- Operationally Compatible with Existing Megabit EPROMs
- Industry Standard 32-pinDual-in-line Package
- All inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Time
- 8-Bit Output for Use in Microprocessor-Based Systems
- Power Saving CMOS Technology
- 3-State Output Buffers
- 400 mV Minimum DC Noise Immunity with Standard TTL Loads
- Latchup Immunity of 250mA on all input and output pins
- No pull-up resistors required
- Low power dissipation (Vcc = 5.5V)
  - Active 165mW Worst case
  - Standby 0.55mW Worst case (CMOS-Input levels)

100Hz FEATURE BOX

VPC3215, CIP3250, SDA9400, DDP3310

The feature box consists of four I2C controlled ICs:

Video Processor	VPC3215
Component Interface Processor	CIP3250
Digital Image Processor	SDA9400
Digital Deflection Processor	DDP3310

The input supplies to the feature box are +12V, +5V. The ICs do also need a supply of 3.3V, which is regulated by IC4 LM314.

Besides the composite video in normal operation and luma/chroma inputs in the SVHS applications, there are also R-G-B-FB inputs from the PIP module.

OSD R-G-B-FB inputs from the Megatext IC or from the controller in the case of TV-text option. While the 50Hz sync signals for PIP are supplied by the VPC3215, the 100Hz sync signals for OSD are supplied by the DDP3310.

Control signals for HV stage such as VertQ, Vert, HDrive, EW (East-West) and SVM (Scan Velocity Modulation) are produced by this module. VProt and HProt input signals are used for protection. There are also a flyback sample signal from HV stage and the sense signal from the CRT board.

The feature box also supports the VGA mode.

VPC32X5 (Video Processor)

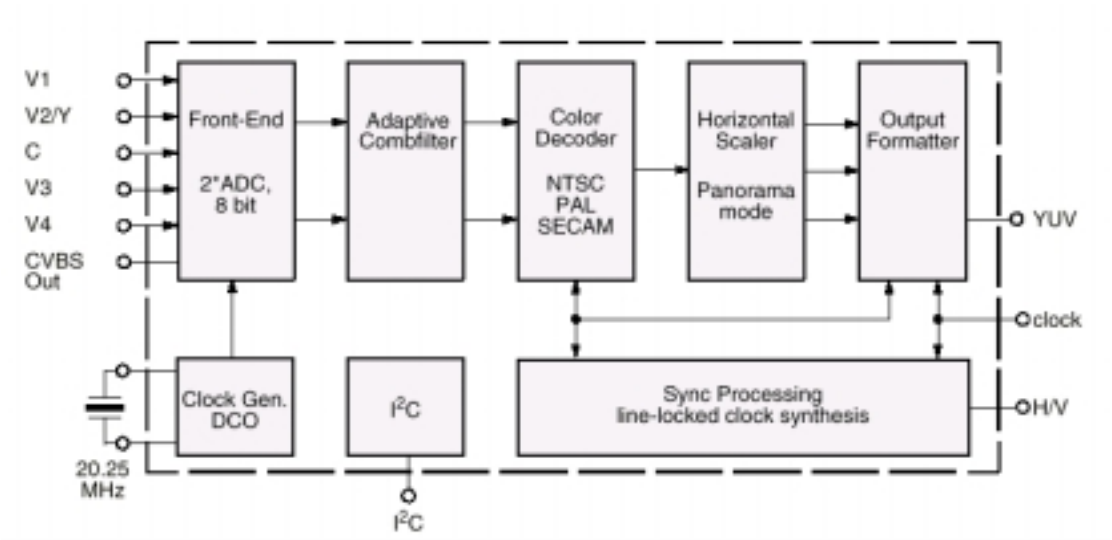


Figure 1

As seen in figure 1 all the processings in VPC are digital. This IC has four composite, one SVHS input, and one composite output which is used for teletext. In AK28 the main video input is Vin2, which is also used for luma input in SVHS applications. After switching the inputs the signals are converted to digital via two 8 bit ADCs. And these digital data are processed to produce the 4:2:2 formatted digital YUV signals. The main features are, multi-standard color decoding including all sub-standards, multi-standard sync processing, adaptive 4H comb filter, linear horizontal scaling, as well as nonlinear horizontal scaling (panorama vision.) It provides 50Hz vertical and 15625Hz horizontal sync signals for the PIP module.

Features:

- all-digital video processing
- high-performance adaptive 4H comb filter Y/C separator with adjustable vertical peaking
- multi-standard color decoder PAL/NTSC/SECAM including all substandards
- 4 composite, 1 S-VHS input, 1 composite output
- integrated high-quality A/D converters and associated clamp and AGC circuits
- multi-standard sync processing
- linear horizontal scaling (0.25 ... 4), as well as non-linear horizontal scaling ‘panorama vision’
- PAL+ preprocessing (VPC 3215)
- line-locked clock, data and sync output (VPC 3215)
- display/deflection control (VPC 3205)
- submicron CMOS technology
- I2C-Bus Interface
- one 20.25 MHz crystal, few external components
- 68-pin PLCC package

Pinning:

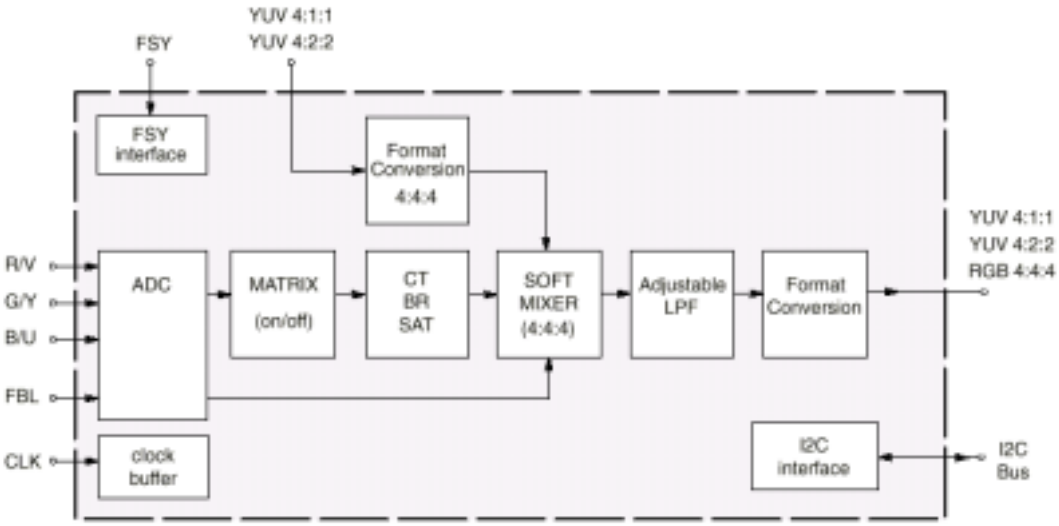
1 Ground
2 Ground
3 5 MHz Clock Out
4 Standby Supply Volt
5 Analog Crystal Out
6 Analog Crystal In
7 Ground
9 Ground
10 Interlace Out
12 Vertical Sync Pulse
13 Front Sync Pulse
14 Main Sync/Horiz Sync Pulse
15 Helper Line Output
16. Horz Clamp Pulse
17. Active Video Out
18. Double Output Clock
19. Output Clock
20...29. Picture Bus Luma
26. Ground
27. Not Connected
30. Main Clock Output 20.25 MHz
31. Supply Volt
34. Ground
35. Ground
36. Supply Voltage
38…47. Picture Bus Chroma
48…50. Picture Bus Priority
51. Ground
52. VGAV Input
53. Front-End/ Back-End Data
54. Reset Input, Active Low
55. I2C Bus Data
56. I2C Bus Clock
57. Test Pin, connect to GND
58. Video 4 Analog Input
59. Ground
60. Video 3 Analog Input
61. Video 2 Analog Input
62. Video 1 Analog Input
63. Chroma/ Video 4 Analog Input
64. Analog Video Output
65. Analog Shield GND F
66. Supply Voltage, Analog Front-End
67. Signal Ground for Analog Input
68. Reference Voltage Top, Analog

CIP3250:

The IC is used to interface the analog input, which is output from the PIP module (SCART RGB or PIP RGB). As can be seen from the block diagram, there is a CT-BR-SAT block, which is used for luma contrast, brightness, hue, and color saturation correction. The soft mixer is controlled by the fast blank signal.

Features:

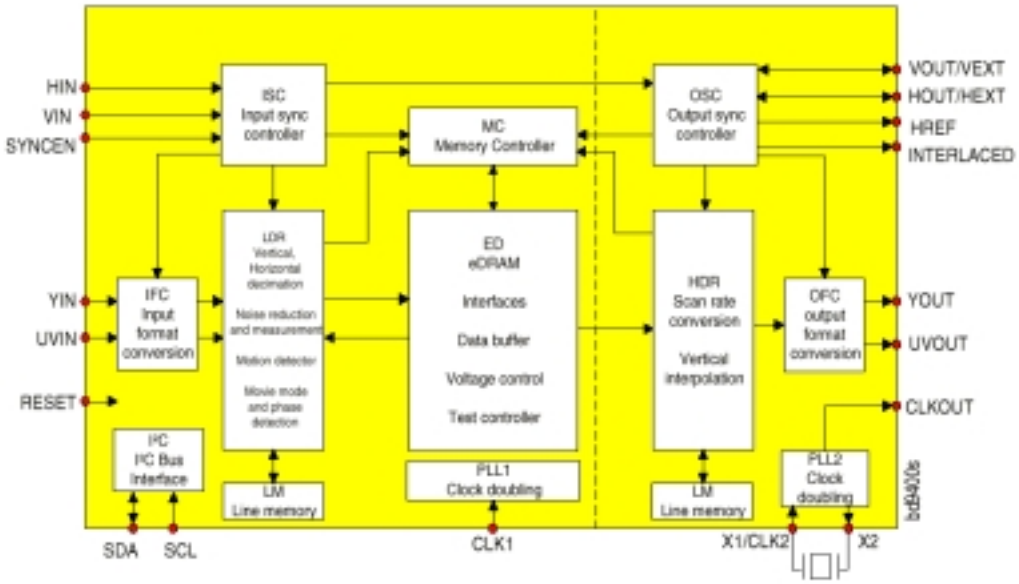
- analog input for RGB or YUV and Fast Blank
- triple 8 bit analog to digital converters for RGB/YUV with internal programmable clamping
- single 6 bit analog to digital converter for Fast Blank signal
- digital matrix RGB % YUV (Y, B–Y, R–Y)
- luma contrast and brightness correction for signals from analog input
- color saturation and hue correction for signals from analog input
- digital input for DIGIT 2000 or DIGIT 3000 formats
- digital interpolation to 4:4:4 format
- high quality soft mixer controlled by Fast Blank signal
- programmable delays to match digital YUVin and ana-log RGB/YUV
- variable low pass filters for YUV output
- digital output in DIGIT 2000 and DIGIT 3000 formats, as well as RGB 4:4:4
- I2C bus interface
- clock frequency 13.5... 20.25 MHz



Pinning:

1. Standby connect to ground
2…9. Blue Output
10…17. Green/Luma Output
18. Pad Ground
19. Pad Supply Voltage +5 V/+3.3 V
20…27. Red/Chroma Output
28. Active Video Output
29. Active Video Input
30. Front Sync Input
31. I2C Clock Input/Output
32. I2C Data Input/Output
33…35. Picture Bus Priority
36…43. Chroma Input
44…51. Luma Input
52. Digital Ground
53. Digital Supply Voltage +5 V
54. Main Clock Input
55. Reset Input
56. In Test Mode connect to ground
57. Analog Supply Voltage +5 V
58. Analog Ground
59. Reference External Capacitor
60. Substrate connect to ground
61. Fast Blank Input
62. Ground Fast Blank
63. Blue/U Input
64. Ground Blue/U
65. Green/Luma Input
66. Ground Green/Luma
67. Red/V Input
68. Ground Red/V

SDA9400:



SDA9400 converts the scan rate from 50/60 Hz to 100/120 Hz

Features:

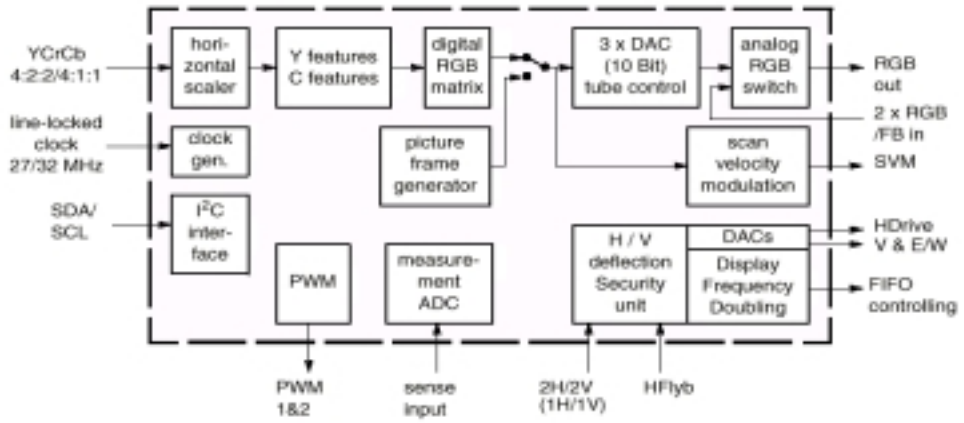
- **Two input data formats**
  -4:2:2 luminance and chrominance parallel (2 x 8 wires)
  -ITU-R 656 data format (8 wires)
- **Two different representations of input chrominance data**
  -2‘s complement code
  -Positive dual code
- **Flexible input sync controller**
- **Flexible compression of the input signal**
  -Digital vertical compression of the input signal (1.0, 1.25, 1.5, 1.75, 2.0, 3.0, 4.0)
  -Digital horizontal compression of the input signal (1.0, 2.0, 4.0)
- **Noise reduction**
  -Motion adaptive spatial and temporal noise reduction (3D-NR)
  -Temporal noise reduction for luminance frame based or field based
  -Temporal noise reduction for chrominance field based
  -Separate motion detectors for luminance and chrominance
  -Flexible programming of the temporal noise reduction parameters
  -Automatic measurement of the noise level (5 bit value, readable by I²C bus)

- **3-D motion detection**
  -High performance motion detector for scan rate conversion
  -Global motion detection flag (readable by I²C bus)
  -Movie mode and phase detector (readable by I²C bus)
- **TV mode detection by counting line numbers (PAL, NTSC, readable by I²C bus)**
- **Embedded memory**
  -5 Mbit embedded DRAM core for field memories
  -192 kbit embedded DRAM core for line memories
- **Flexible clock and synchronization concept**
  -Decoupling of the input and output clock system possible
- **Scan rate conversion**
  -Motion adaptive 100/120 Hz interlaced scan conversion
  -Motion adaptive 50/60 Hz progressive scan conversion
  -Simple static interlaced and progressive conversion modes for 100/120 Hz interlaced or 50/60 Hz progressive scan conversion : e.g. ABAB, AABB, AA*B*B, AAAA, BBBB, AB, AA*
  -Simple progressive scan conversion with joint lines:
  50 Hz -> 60, 70, 75 Hz progressive
  60 Hz -> 70, 75 Hz progressive
  -Large area and line flicker reduction
- **Flexible digital vertical expansion of the output signal (1.0, ... [1/32] ... , 2.0)**
- **Flexible output sync controller**
  -Flexible positioning of the output signal
  -Flexible programming of the output sync raster
  -External synchronization by backend IC possible
  (e.g. split screen for one TV channel with joint lines and one PC VGA channel)
- **Signal manipulations**
  -Insertion of coloured background
  -Vertical and/or horizontal windowing with four different speed factors
  -Flash generation (for supervising applications, motion flag readable by I²C bus)
  -Still frame or field
  -Support of split screen applications
  -Multiple picture display - Tuner scan (4 and 16 times for 4:3, 12 times for 16:9 tubes)
  -Support of multi picture display with PIP or front-end processor with integrated scaler
  (e.g. 9 times display of PIP pictures, picture tracking, random pictures, still-in-moving picture, moving-in-still picture)
- **I²C-bus control (400 kHz)**
- **3.3 V ± 5% supply voltage**

Pinning:

2,8,24,42,55	Supply volt (*V*SS=0V)	54.	System clock 1
9,25,41,56	Supply volt (*V*DD=3.3V)	17,..,10	Data output UV
36,52,58	Supply volt (*V*SS=0V)	7,..,3;1;64;63	Data output Y
35,51,53,57,59	Supply volt (*V*DD=3.3V)	62	Horz active video out
43,..,50	Data input Y	61	V-Sync out / Ext V-Sync
31,..,34;37,..,40	Data input UV	60	H-Sync out / Ext H-Sync
30	System reset.	18	Interlace signal vert deflection
23	H-Sync input	28	Crystal conn / System clock 2
22	V-Sync input	27	Crystal connection
29	Sync enable input	26	Clock output
21	I2C-Bus data line	19	Test input
20	I2C-Bus clock line		

DDP3310:



It is the display and deflection processor. All the horizontal and vertical stages are driven by this IC.
The last controls such as contrast, brightness and saturation of the actual video signal, OSD and VGA are accomplished by the blocks in DDP. Tube measurement and SVM controls are also managed by this IC.

Features:

Video processing

– linear horizontal scaling (0.25 … 4)
– non-linear horizontal scaling “panoramavision”
– dynamic peaking
– soft limiter (gamma correction)
– color transient improvement
– programmable RGB matrix
– picture frame generator
– two analog RGB/Fast-Blank inputs

Deflection processing

– scan velocity modulation output
– high-performance H/V deflection
– EHT compensation for vertical / East/West
– soft start/stop of H-Drive
– vertical angle and bow
– differential vertical output
– vertical zoom via deflection
– horizontal and vertical protection circuit
– adjustable horizontal frequency for VGA/SVGA dis-play

Miscellaneous

– selectable 4:1:1/ 4:2:2 YC r C b input
– selectable 27/ 32-MHz line-locked clock input
– crystal oscillator for horizontal protection
– automatic picture tube adjustment (cutoff, white-drive)
– single 5-V power supply
– hardware for simple 50/60-Hz to 100/ 120-Hz con-version (display frequency doubling)
– two I2C-controlled PWM outputs
– beam current limiter

Pinning:

1. Supply Voltage
2. Gnd, Output Pin Driver
3. Additional VSYNC input
4. Read counter Reset
5. FIFO Read Enable
6. FIFO Write Enable
7. FIFO Write counter Reset
8. Horz. Drive Output
9. Horz. Flyback Input
10. Safety Input
11. Vertical Protection Input
12. Select of H-Drv Freq. Range
13. Clock Sel 40.5 or 27/32MHz
14. Clock select 27/32 MHz
15. Range Switch2, Measure ADC
16. Range Switch1, Measure ADC
17. Sense ADC Input
18. Ground, MADC Input
19. Differential Vert Sawtooth Out
20. Differential Vert Sawtooth Out
21. E/W Output
22. Reference Input for RGB DACs
23. Scan Velocity Modulation
24. Analog Output Red
25. Analog Output Green
26. Analog Output Blue
27. Ground, Analog Back-end
28. Sup Volt, Analog Back-end
29. VRD/BCS DAC Ref, Beam Current Safety
30. Fast-Blank1 Input
31. Analog Red1 Input
32. Analog Green1 Input
33. Analog Blue1 Input
34. Fast-Blank2 Input
35. Analog Red2 Input
36. Analog Green2 Input
37. Analog Blue2 Input
38. Test Pin
39. Reset Input, active low
40. PWM out
41. PWM out
42. Half-Contrast

43…50. Picture Bus Chroma

51. Supply Volt, Digital Circuitry
52. Ground, Digital Circuitry
53. Sys. Clock Input(27/32/40.5MHz)

54…61. Y0 Picture Bus Luma

62. Single LLC Input(13.5/16MHz)
63. Horizontal Sync Input
64. Vertical Sync Input
65. Analog Crystal Out (5-MHz Security Clock)
66. Analog Crystal In (5-MHz Security Clock)
67. I2C-Bus Data
68. I2C-Bus Clock

AK28 CHASSIS MANUAL ADJUSTMENTS PROCEDURE

A) PRELIMINARY

Before starting with the alignment procedure, make sure that all the potentiometers on the chassis and also screen and focus pots are in the medium position.

B) SYSTEM VOLTAGE ADJUSTMENT

Inputs - AC power (220V 50 Hz).
- PAL B/G test pattern via RF
(PAL I test pattern for PAL I TV's, SECAM D/K pattern, SECAM L/L´/K´ TV's).

Outputs - Digital voltmeter to anode of D110.

Display - System voltage

Action - Apply power. Check that The stand-by led lights.
- Select TV mode and tune to the applied test pattern via local test keyboard. Chassis should start normally.
- Adjust all analogue controls (volume, bass, treble, brightness, contrast, colour) to minimum settings.
- Adjust VR127 according to the following different types of CRT's

SYSTEM VOLTAGE	TYPE OF CRT
135V±0.5V	PHILIPS A66EAK552X54
135V±0.5V	PHILIPS A66EAK071X54
135V±0.5V	VIDEOCOLOR A66ECY13X12
135V±0.5V	PHILIPS W66ESF002X44

C) AFC ADJUSTMENT

Inputs - AC power.
- 38.9 MHz test pattern for PAL B/G, PAL-SECAM B/G or 39.5 MHz test pattern for PAL I model (90dBmV) to Z403 SAW filter input terminals 1 and 2.

Outputs - Digital Voltmeter to AFC point (pin22 of IC401)

Display - AFC Voltage.

Action - Adjust VL401 for 2.5±0.1 Volts. TV should automatically tune to a station when search tuning is activated.

D) FOCUS ADJUSTMENT

Inputs - AC power
- PAL B/G test pattern via RF input.

Outputs - Picture tube drive.

Display - Picture

Action - Select TV mode and tune to the signal.
- Adjust focus potentiometer (the upper pot on the rear side of the FBT transformer) for optimum focusing.drive.

E) SCREEN ADJUSTMENT

Inputs - AC power
- PAL B/G Colour Bar test pattern via RF

Outputs - 1/100 Oscilloscope probe to RGB cathodes on CRT baseboard.
NOTE:Ground pin of probe will be connected to 1st pin (GND) of the CRT socket.

Display - RGB ratio

Action - Select PAL B/G Colour Bar pattern using the local test keyboard and the user remote control unit.
- Adjust all control functions (brightness, colour and contrast) to minimum settings.
- Measure the most sensitive cathode
- Adjust the screen potentiometer (lower pot on the rear side of FBT transformer) until cathode voltage becomes 150V.

F) IF ADJUSTMENT FOR L' MODE

Inputs - AC power.
- 38.9 MHz test pattern for PAL B/G, PAL-SECAM B/G or 39.5 MHz test pattern for PAL I model. (90dBmV) to Z403 SAW filter input terminals 1 and 2.

Outputs - Digital Voltmeter to AFC point. (pin22 of IC401)
- Digital Voltmeter to AFC_L point. (pin14 of IC401)

Display - AFC Voltage.

Action - Firstly adjust VL401 for 2.5 ± 0.1 Volts. TV should automatically tune to a station. when search tuning is activated.
- Adjust VR401 for 2.5±0.1 Volts at the AFC_L point.

AK28 CHASSIS PRODUCTION MODE ADJUSTMENTS PROCEDURE

A) PRELIMINARY

All system, geometry and white balance alignments are performed in production service mode. Before starting the production mode alignments, make sure that all manual alignments are done correctly. To start production mode alignments enter the MAIN MENU and enter the code **1675** by pressing digit keys. Production mode items will appear on the screen. Production mode groups will be displayed with different colours of headlines , so in order to access a production alignment group press the colour key of the related group on the remote control transmitter. After selecting one of the production service mode groups, you can access its items by pressing the cursor-up and/or cursor-down keys. You can change the value of an item by pressing cursor-left and/or cursor-right keys on the remote control transmitter.
In order to switch between other group of items press the colour key of this groups headline.
To store the settings press OK key. In order to leave this menu press MENU key.

B) HORIZONTAL AND VERTICAL GEOMETRY ALIGNMENTS

- Switch the program to crosshatch test pattern.
- Press RED key to access this group of item.
- Select the items by pressing cursor-up and/or cursor-down keys.
- Adjust the item by pressing cursor-left and/or cursor-right after selecting that item.
- Store the settings by pressing OK key.
- Switch to another item group by pressing the colour keys of the related coloured headline of that group.
- Exit production mode by pressing the MENU key on the remote transmitter..

1) V-SHIFT
- Press cursor-left and/or cursor-right buttons till the test pattern is vertically centred, i.e. horizontal line at the centre of the test pattern is in equal distance both to upper and lower side of the picture tube. Check and readjust V-SHIFT item if the adjustment becomes improper after some other geometric adjustments are done

2) V-SIZE
- Press cursor-left and/or cursor-right buttons till horizontal black lines on both the upper and lower part of the test pattern become very close to the upper and lower horizontal sides of picture tube and nearly about to disappear. Check and readjust V-SIZE item if the adjustment becomes improper after some other geometric adjustments are done.

3) H-SHIFT
- Adjust H-SHIFT item by pressing cursor-left and/or cursor-right buttons till test pattern is horizontally in equal distance both to right and left sides of the picture tube. Check and readjust H-SHIFT item if the adjustment becomes improper after some other geometric adjustments are done.

4) H-SIZE
- Adjust H-WIDTH item by pressing cursor-left and/or cursor-right buttons till no under-scan condition will happen, i.e. no white bars on the left and right side of the test pattern will be visible nor the picture will be so wide. Check and readjust H-WIDTH item if the adjustment becomes improper after some other geometric adjustments are done.

5) S-COR
- Press cursor-left and/or cursor-right buttons till the size of squares on both the upper and lower part of test pattern become equal to the squares laying on the vertical centre of the test pattern. Check and readjust S-COR item if the adjustment becomes improper after some other geometric adjustments are done.

6) LINRT
- Press cursor-left and/or cursor-right buttons till all the size of squares of the test pattern become in equal size from the top of the screen to its bottom of the whole screen. Check and readjust LINRT item if the adjustment becomes improper after some other geometric adjustments (especially after than S-COR adjustment are done.

7) ANGLE
- Press cursor-left and/or cursor-right buttons till the vertical lines of the crosshatch pattern become completely perpendicular to horizontal lines without any angle of vertical deviation. Check and readjust ANGLE item if the adjustment becomes improper after some other geometric adjustments are done.

8) BOW
- Press cursor-left and/or cursor-right buttons till the vertical lines especially ones close to the left and right sides will of equal and symmetrical bending, i.e. they together will neither be towards left side nor right side. Check and readjust BOW item if the adjustment becomes improper after some other geometric adjustments are done.

9) TRPEZ
- Press cursor-left and/or cursor-right buttons till vertical lines, especially lines at the sides of the picture frame became parallel to the both sides of picture tube as close as possible. Check and readjust TRPEZ item if the adjustment becomes improper after some other geometric adjustments are done.

10) PARAB
- Press cursor-left and/or cursor-right buttons till vertical lines close to the both sides of the picture frame become parallel to vertical sides of picture tube without any bending to left or to right side of the screen.. Check and readjust PARAB item if the adjustment becomes improper after some other geometric adjustments are done.

11) U. COR

- Press cursor-left and/or cursor-right buttons till vertical lines at the upper corners of the picture frame become vertical and parallel to vertical corner sides of picture tube. Check and readjust U. COR item if the adjustment becomes improper after some other geometric adjustments are done.

12) L. COR

- Press cursor-left and/or cursor-right buttons till vertical lines at the lower corners of the picture frame become vertical and parallel to vertical corner sides of picture tube. Check and readjust L. COR item if the adjustment becomes improper after some other geometric adjustments are done.

C) VIDEO ALIGNMENTS

- Switch the program to crosshatch test pattern for geometric adjustments.
- Switch the program to colour bar test pattern for video adjustments.
- Press GREEN key to access this group of item.
- Select the items by pressing cursor-up and/or cursor-down keys.
- Adjust the item by pressing cursor-left and/or cursor-right after selecting that item.
- Store the settings by pressing OK key.
- Switch to another item group by pressing the colour keys of the related coloured headline of that group.
- Exit production mode by pressing the MENU key on the remote transmitter..

1) RGn, GGn, BGn: WHITE BALANCE ADJUSTMENT

- Apply WHITE test pattern via RF.

Adjust all analogue functions to medium level and set GGn, RGn, BGn at value 80, if needed.
Use Colour analyser and monitor the colour temperature (X, Y) on colour analyser.
Select RGn and BGn by cursor-up and/or cursor-down buttons and change the values by cursor-left and/or cursor-right buttons till the following values are read:

X=285±10
Y=293±10 on the colour analyser.

2) RRf, GRf, BRf

Set the values of these items as 62 (constant).

3) YDF

Apply COLOUR BAR test pattern.
Select YDF item cursor-up and/or cursor-down buttons.
Adjust YDF by pressing cursor-left and/or cursor-right buttons till the colour transients on the colour bar pattern becomes as sharper and possible as colours between transients do not mix with each other. Check and readjust YDF item if the adjustment becomes improper after YDV adjustment is done.

4) AGC

Apply PAL BG signal, VHF-3 Channel-12 and 60dBmV RF signal level.
Adjust AGC item till voltage at the AGC point (pin1 of the tuner) becomes 3.0 volts.

5) TLAN

This item and its settings will be defined later.

6) APS

This value of this item toggles between ON and OFF while pressing the cursor-left and cursor-right after this item is selected by cursor-up and/or cursor-down buttons.
In order to activate APS installation procedure whenever TV is turned select ON for the very first time.
In order to start TV without APS installation procedure select OFF.

7) T_T

This item is used for the Tuner Selection.
SAM, THO, SIE, ALP, MK2 and MK3 are for Samsung, Thomson, Siemens, Alps and Philips MP2/MP3, respectively.

8) T_P

This item is used for the Tuner Selection.
SAM, THO, TEM, and MK2 are for Samsung, Thomson, Temic, and Philips, respectively.

9) EXT3

This item is toggles between ON and OFF and is used to enable and disable EXT3, respectively.

10) CLT

This item is used to set the Menu colors. 5 choices are possible.

D) SERVICE ALIGNMENTS

IMPORTANT: There will no adjustments in this service mode during production mode alignments.

- Press BLUE key on the remote transmitter when Production mode is active.
- Press the colour key of the related item group's headline colour
- Press cursor-up and/or cursor-down to select the item of the group
- Press cursor-left and/or cursor-right to alter the value of the item.
- Press OK to store the values of items and MENU to exit the service alignments mode.

1) ADJUSTMENTS GROUP

Press RED key on the remote transmitter in order to access this group of items.

PIP CNTRST , level of the PIP picture
PIP YDelay , luma delay of the PIP picture
PIP Frame , color selection of the PIP frame. (edges of the PIP)
EHTHP , EHT compensation coefficient for horizontal phase
EHTH TC , EHT time contant for horizontal phase compensation
EHTH , EHT compensation coefficient for horizontal amplitude
EHTV , EHT compensation coefficient for vertical amplitude
EHTV TC , time contant for control of vertical and horizontal amplitude EHT compenzation. (0 means off.)
OSD LEVEL , contast level of the OSD
INIT NVM , to initiate the NVM

2) OPTIONS GROUP

- Press BLUE key on the remote transmitter in order to access this group of items.

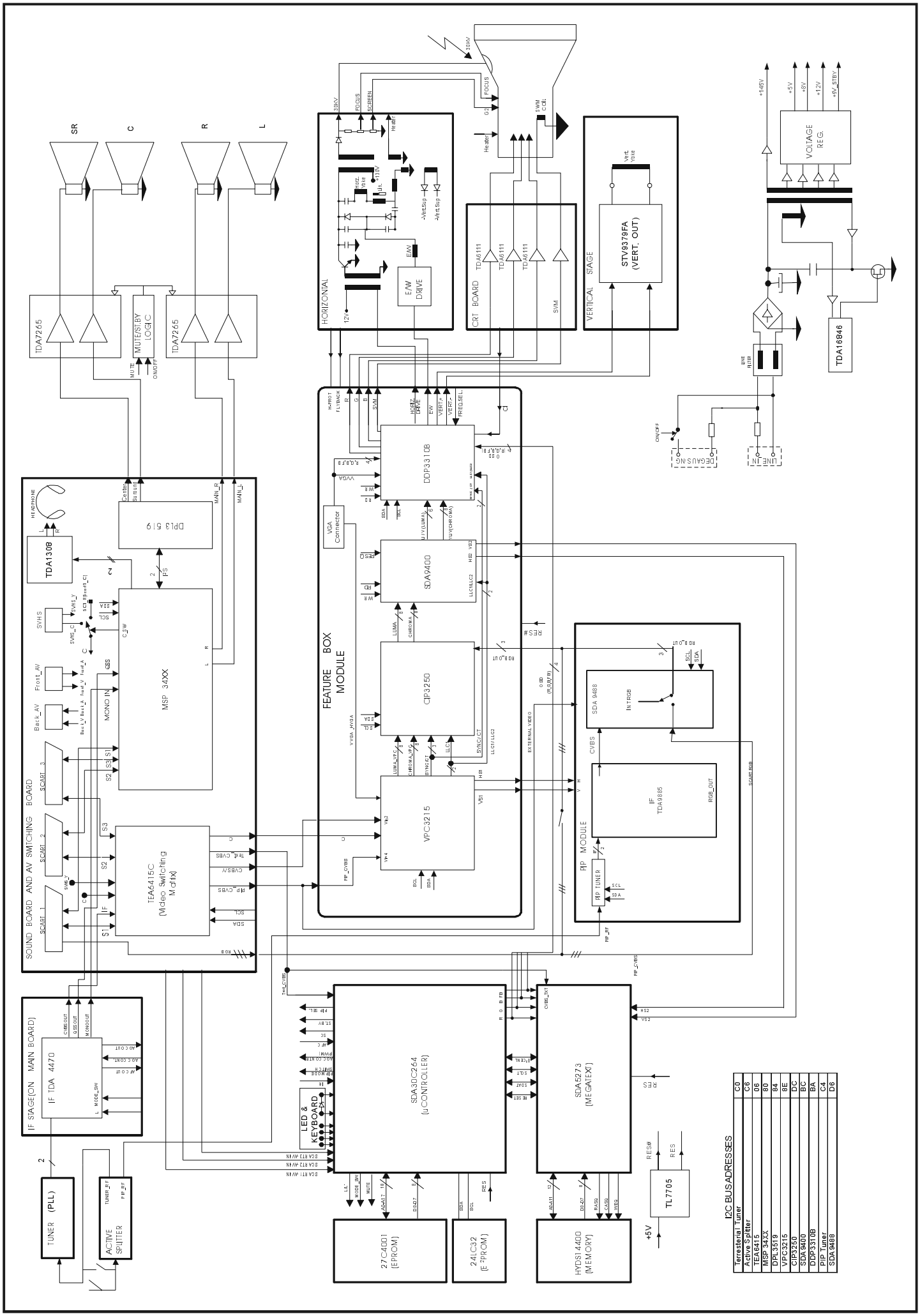
0. HPHONE , on / off
1. CRT , 4:3 / 16:9
2. S-VHS , on / off
3. f(IF) , always set to 38.9
4. Türk. , turkish menu on/off
5. VGA , on / off
6. FRONT , Front AV on/off

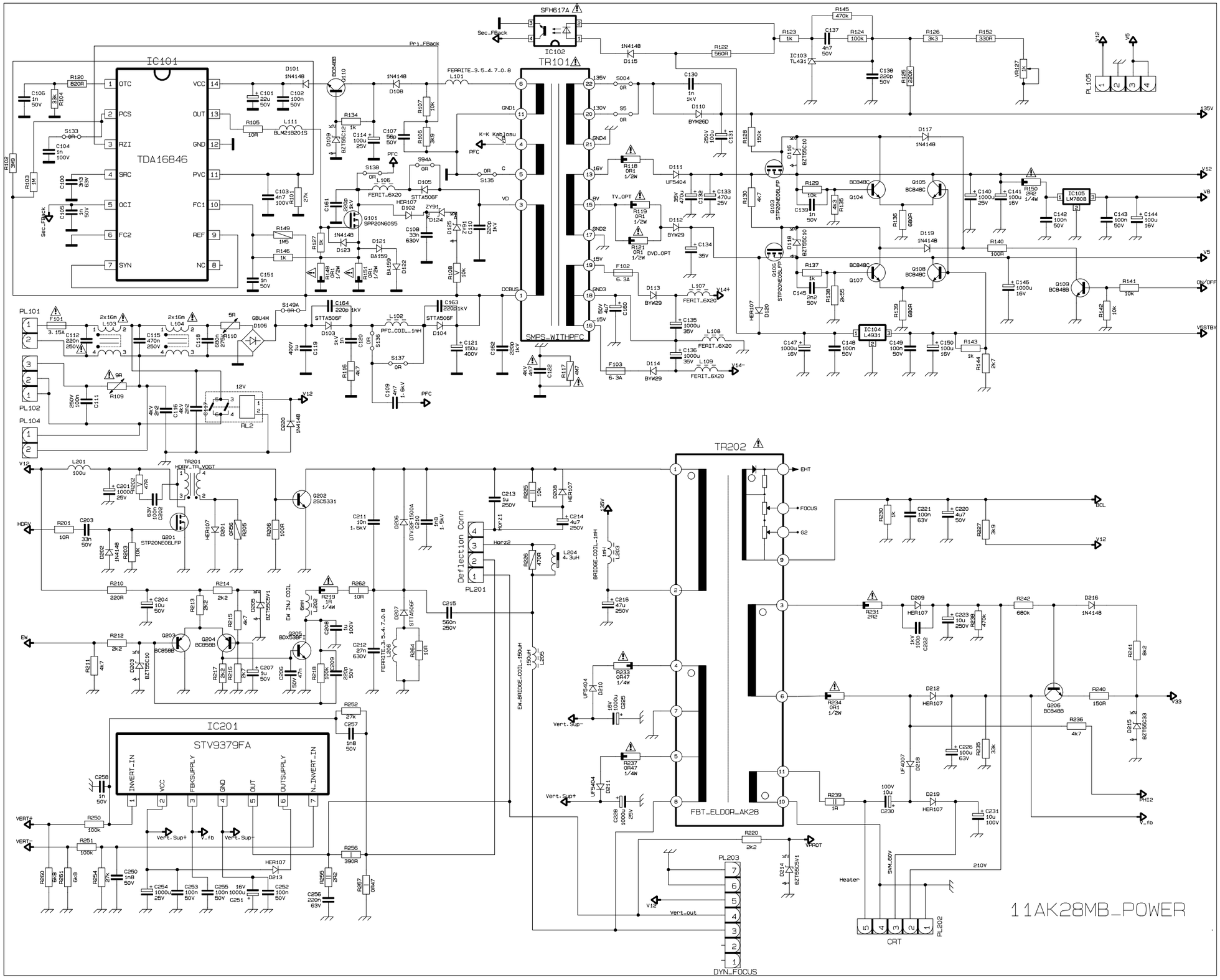
3) SYSTEM GROUP

- Press YELLOW key on the remote transmitter in order to access this group of items.

0. PAL B/G , on / off
1. PAL D/K , on / off
2. PAL I , on / off
3. SECAM B/G , on / off
4. SECAM D/K , on / off
5. SECAM L/L' , on / off
6. AUST. , on / off

GENERAL BLOCK DIAGRAM OF CHASSIS AK28

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SYN
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OUT
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NC
SFH617A
IC102
TR101
SMPS_WITHPFC
FERRITE_3.5_4.7_0.8
K-K Kablosu
Deflection Conn
PL201
IC103
TL431
IC104
L4931
IC105
LM7808
PL105
PL101
PL102
PL104
PL203
DYN_FOCUS
PL202
CRT
TR202
FBT_ELDOR_AK28
IC201
STV9379FA
INVERT_IN
VCC
FBKSUPPLY
GND
OUT
OUTSUPPLY
N_INVERT_IN
TR201
HDRV_TR_VOGT
RL2
Q101
SPP20N60S5
Q201
STP20NE06LFP
Q202
2SC5331
Q203
BC858B
Q204
BC858B
Q205
BDX53BFP
Q103
STP20NE06LFP
Q105
STP20NE06LFP
Q104
BC848C
Q105
BC848C
Q107
BC848C
Q108
BC848C
Q206
BC848B
Q109
BC848B
135V
V12
V8
V5
ON/OFF
VSTBY
V14+
V14-
V33
PHI2
V_fb
EHT
FOCUS
G2
BCL
VPROT
Heater
SVM_60V
210V
Vert.Sup+
Vert.Sup-
V_fb
Vert_out
Sec_FBack
Pri_FBack
PFC
DVD_OPT
TV_OPT
DCBUS
EW
HDRV
Horz1
Horz2
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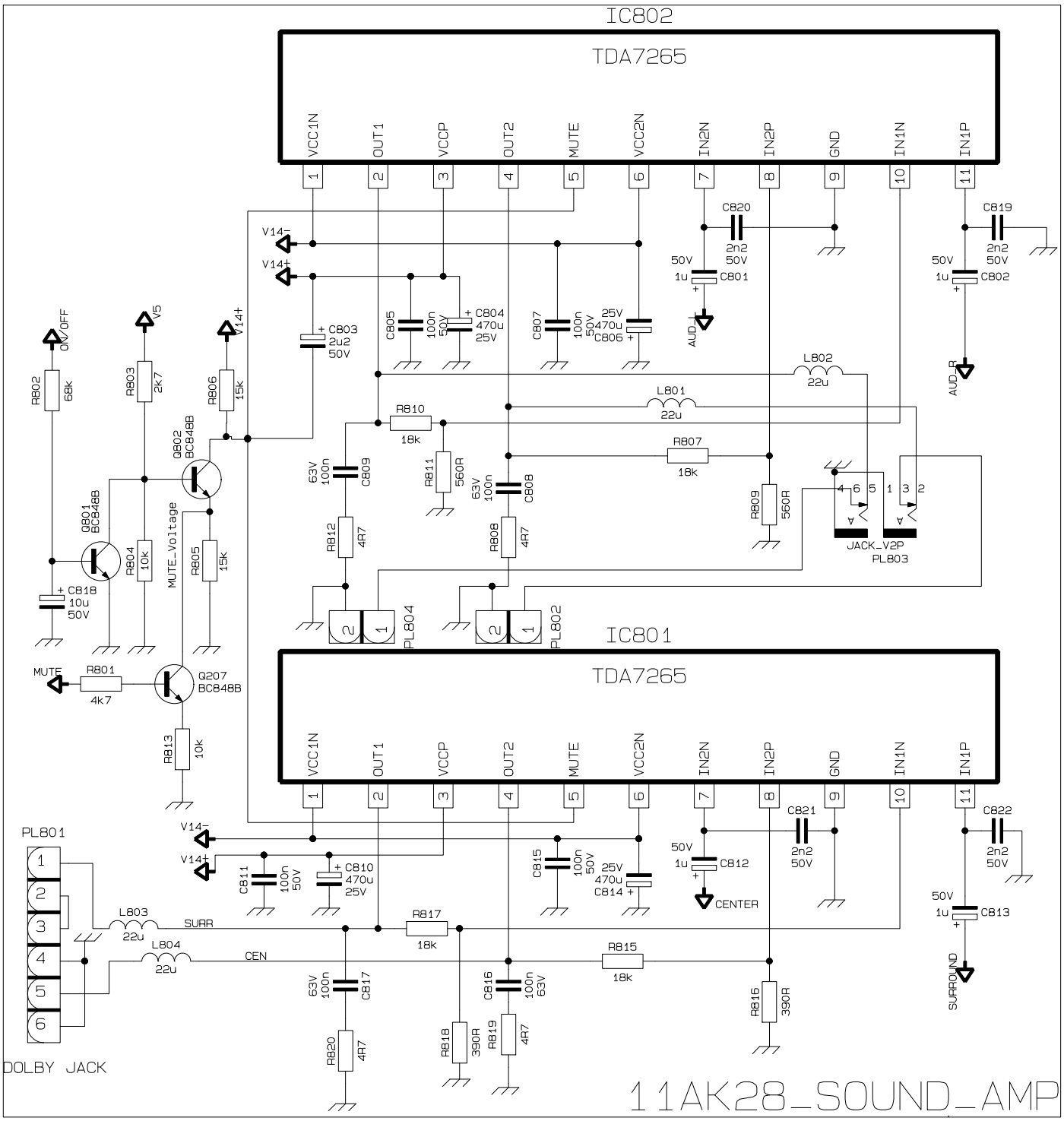
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2n2
50V
C819
2n2
50V
50V
1u
C801
50V
1u
C802
AUD_L
AUD_R
V14-
V14+
C803
2u2
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C805
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100n
50V
25V
470u
C806
L802
22u
L801
22u
R810
18k
R807
18k
R802
68k
ON/OFF
R803
2k7
V5
R806
15k
V14+
Q802
BC848B
63V
100n
C809
R811
560R
63V
100n
C808
R809
560R
R812
4R7
R808
4R7
Q801
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50V
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CENTER
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SURROUND
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L804
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R815
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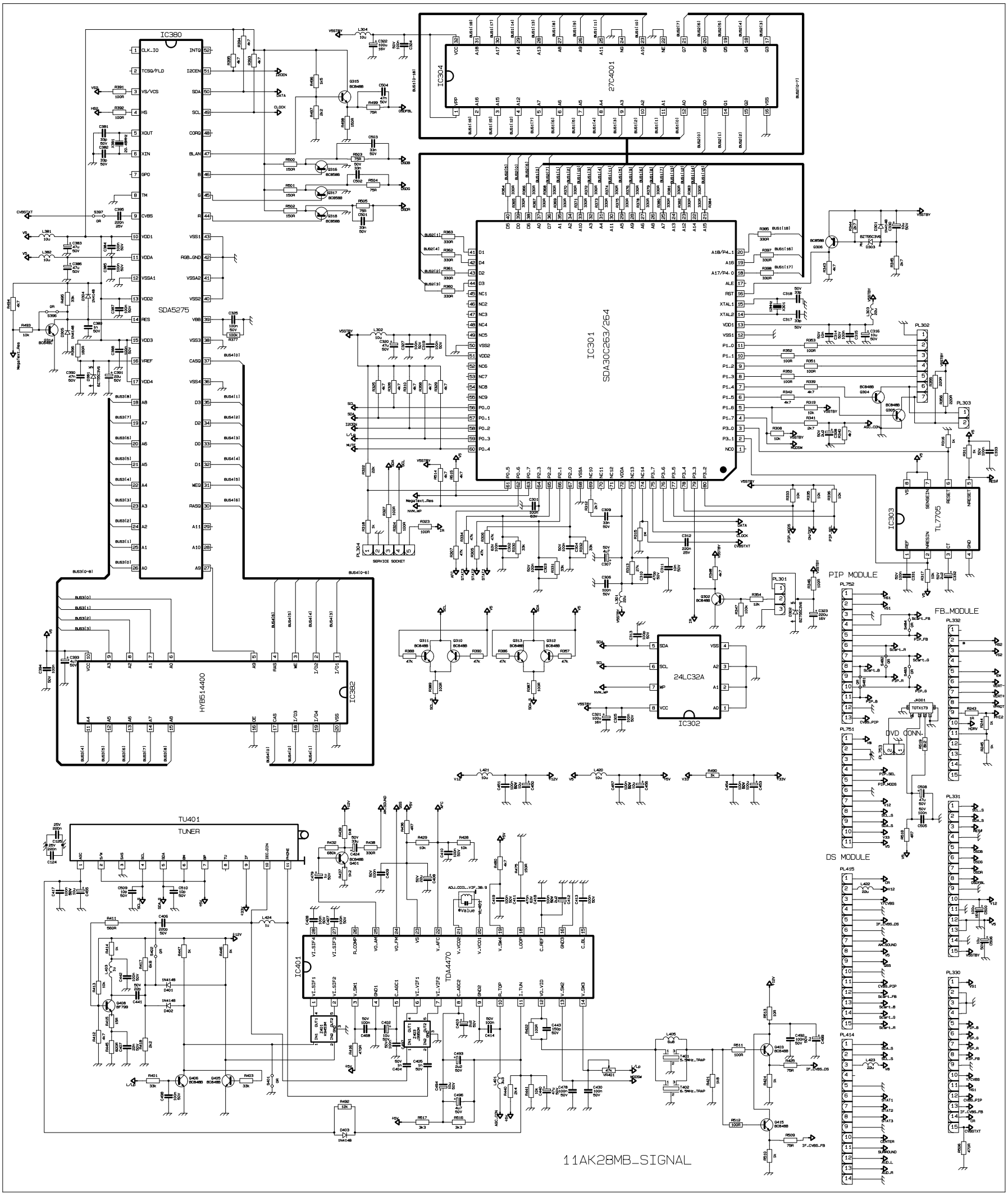
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TUNER
IC401
TDA4470
PIP MODULE
FB_MODULE
DVD CONN.
DS MODULE
SERVICE SOCKET
11AK28MB_SIGNAL